

COURSE OVERVIEW

Full Course Title: Chip Design

Instructional Hours (Contact Hours): 30 Hours

Course Description:

Bring this world to great change of IC's Design concepts of different IP cores including all peripherals in a single chip. These disciplines stay digital design to competitive careers for semiconductor world. Extended course & certification programs combine theoretical knowledge with practical EDA transformation for involving technologies of the future. Goal of this course is to get an ideas on Chip Design concepts and Fabrication Technologies. Students will learn from scratch to new-rich of IC Design concepts.

Learning Outcomes:

- By the end of this course, students will be able to:
- Learn concepts of VLSI Design like CMOS & FinFET technology
- Get idea on HDL languages for the RTL designs
- Gain knowledge about how a chip can be constructed
- Experience Chip Design process & Manufacturing ideas
- Learn Multiple Cores including a Microcontroller, Microprocessor, Digital Signal Processor or an application – specific instruction set processor.

Learning Activities:

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|---|---|
| <input checked="" type="checkbox"/> Class Discussions/Discussion Boards | <input checked="" type="checkbox"/> Student Projects |
| <input checked="" type="checkbox"/> Peer-to-Peer Work (pairs, small groups) | <input checked="" type="checkbox"/> Readings |
| <input checked="" type="checkbox"/> Written Assignments (reports, essays) | <input checked="" type="checkbox"/> Textbook/Workbook Exercises |
| <input checked="" type="checkbox"/> Case Study Analysis | <input type="checkbox"/> Other: Click to enter |

Methods of Assessment/Grading Criteria:

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|---|---|
| <input checked="" type="checkbox"/> Class/Discussion Boards Participation | <input checked="" type="checkbox"/> Individual Projects/Presentations |
| <input checked="" type="checkbox"/> Written Assignments (reports, essays) | <input checked="" type="checkbox"/> Group Projects/Presentations |

COURSE OVERVIEW

Course Topics:

- VLSI, SoC & FPGA Architecture
- Languages- VHDL, System Verilog, Verilog & Chisel
- RTL Design Concepts and Coding Guidelines
- Verification Methodology
- FPGA Programming and Implementation
- EDA Tool (OpenROAD) understanding with LAB Facilities
- Synthesis to GDSII flow using OpenROAD
- Release to Chip Fabrication

Prerequisites:

Previous knowledge of general OOPS Concepts language related Electronics Topic, Transistor, CMOS or equivalent is required before taking this course.